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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,729	10/29/2003	Hoang T. Tran	1875.4520000	4015

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EXAMINER	
SUN, SCOTT C	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
05/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,729	TRAN ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendments to the claims filed 2/16/2007 has been noted and entered.

Response to Arguments

2. Applicant's arguments with respect to claims 12-30 have been considered but are moot in view of the new ground(s) of rejection.

Election/Restrictions

3. This application contains claims 1-11 drawn to an invention nonelected with traverse. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12, 15, 16, 18-20, 25-27 are rejected under 35 U.S.C. 102(e) as being unpatentable Weber et al (PG Pub #2003/0120791) in view of Cliff et al (PG Pub #2001/0017595)

6. Regarding claim 12, Weber discloses a transceiver (system 400 in figure 4), comprising:

a plurality of ports (serializer/deserializers 410-413);

a bus (connections between the various elements in figure 4) connecting said plurality of ports on a common substrate (single die, paragraph 22);

a plurality of programmable pads (data presenters 460-463, and aggregators 440-443 and corresponding encoder/decoders) in communications with said plurality of ports (paragraph 23);

a register (register bits, paragraph 24) for sending instructions to configure at least one of said programmable pads to comply with a specified data protocol (STMS, Fibre, Ethernet, etc) and the specified electrical specification (serial/parallel, different bit rates of each protocol). Examiner notes that Weber discloses the data presenters and aggregators are instructed to process data according to the desired protocol definition and its transfer rate (paragraphs 23-25).

Weber does not disclose explicitly the electrical specifications include configuring an operating voltage. However, Cliff discloses configuring an operating voltage for a programmable logic device (programmable voltage regulator 310, figure 3; paragraph 29, 32). Teachings of Weber and Cliff are from the same field of programmable circuits.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Weber and Cliff by adding programmable voltage regulator into the system of Weber for the benefit of efficiently retrofitting the programmable device (paragraph 29, Cliff).

7. Regarding claim 15, Weber and Cliff combined disclose claim 12 and Weber further discloses an input controller (protocol processors 450-455) for configuring at least one of said programmable pads to receive at least one of a data signal and a control signal (paragraphs 16, 23).

8. Regarding claim 16, Weber and Cliff combined disclose claim 12 and Weber further discloses an output controller (protocol processors 450-455) for configuring at least one of said programmable pads to send at least one of a data signal and a control signal (paragraphs 17-24).

9. Regarding claims 18-20 and 25-27, examiner notes that these claims contain limitations substantially similar to those in claims 12, 15 and 16. The same grounds of rejection are applied.

10. Claims 17, 21, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber in view of Cliff further in view of Rearick et al (PG Pub #2003/0172332).

11. Regarding claim 17, Weber and Cliff combined disclose claim 12 but do not disclose explicitly measuring leakage current. However, Rearick discloses a testing register (driver test system 200, figure 2) for sending a test message to measure leakage current (tri-state leakage current) from at least one of a programmable pad

(paragraphs 33, 40). Teachings of Weber, Cliff and Rearick are from the same field of integrated circuits.

Therefore, it would have been obvious at the time of invention to combine teachings of Weber, Cliff and Rearick by adding the testing circuit to the system of Weber for the benefit of providing cost-effective and accurate self-testing capability to the integrated circuit (background, Rearick).

12. Regarding claims 21 and 28, examiner notes that these claims contain limitations substantially similar to those in claim 17. The same grounds of rejection are applied.

13. Claims 13, 14, 22-24, 29, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber in view of Cliff further in view of Taniguchi et al (PG Pub #2001/0015664).

14. Regarding claim 13, Weber and Cliff combined disclose claim 12 but do not disclose explicitly adjusting a delay between input and output. However, Taniguchi discloses a timing controller (delay adjustment circuit, figure 5) for modulating delay between input (input buffer) and output (output buffer) of an integrated circuit (DLL Array 7; paragraphs 52, 53). Teachings of Weber, Cliff and Taniguchi are from the same field of integrated circuits.

Therefore, it would have been obvious at the time of invention to combine teachings of Weber, Cliff and Taniguchi by using the adjustable delay circuit disclosed

by Taniguchi in the system of Weber for the benefit of underflow and overflow prevention (paragraph 87, Taniguchi).

15. Regarding claim 14, Weber and Cliff combined disclose claim 12, and Taniguchi further discloses a timing register for sending instructions to adjust the delay between input and output of at least one of said programmable pads. Examiner notes that the same reasons to combine the teachings of Weber and Taniguchi can be applied.

16. Regarding claims 22-24, 29-30, examiner notes that these claims contain limitations substantially similar to those in claim 13 and 14 above. The same grounds of rejection are applied. Further regarding claims 23 and 24, Examiner notes that Taniguchi discloses that the data is delayed in a buffer (input/output buffer), where the delay is a fixed time interval set by the delay adjustor circuit (figure 5, paragraphs 9, 52).

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

KIM HUYNH
SUPERVISORY PATENT EXAMINER
5/14/07